

Fig.1

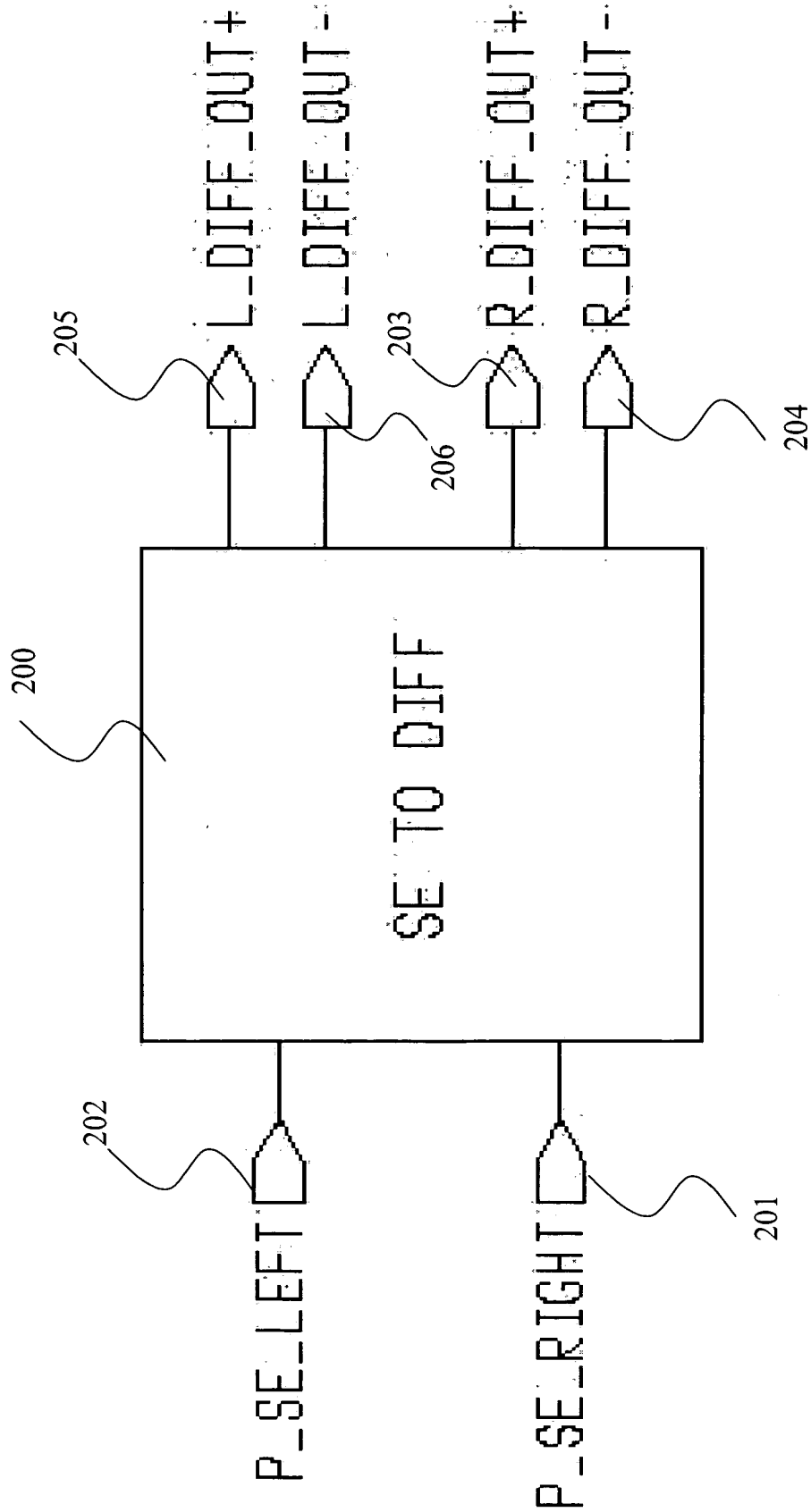


Fig.2

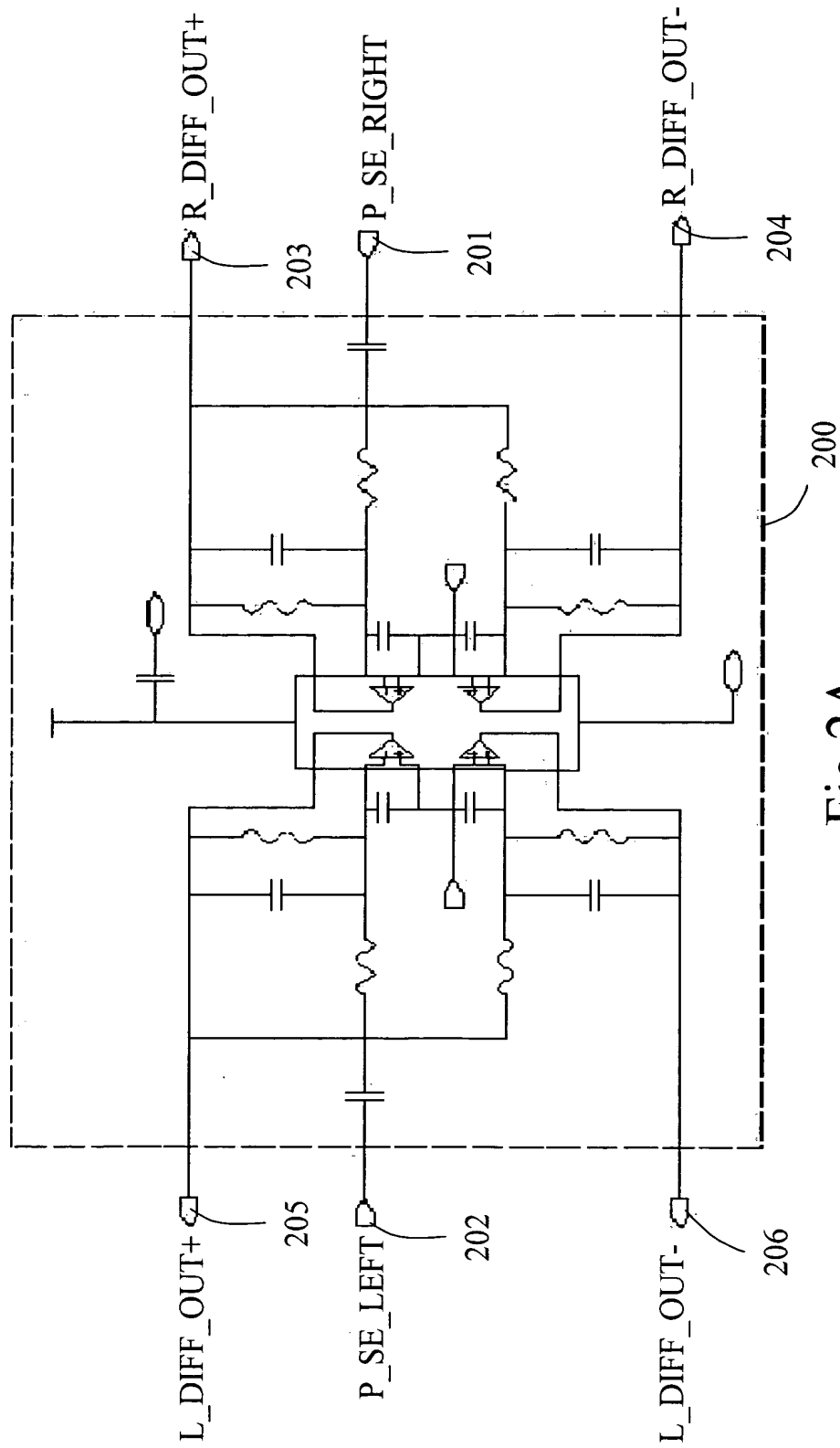


Fig.2A

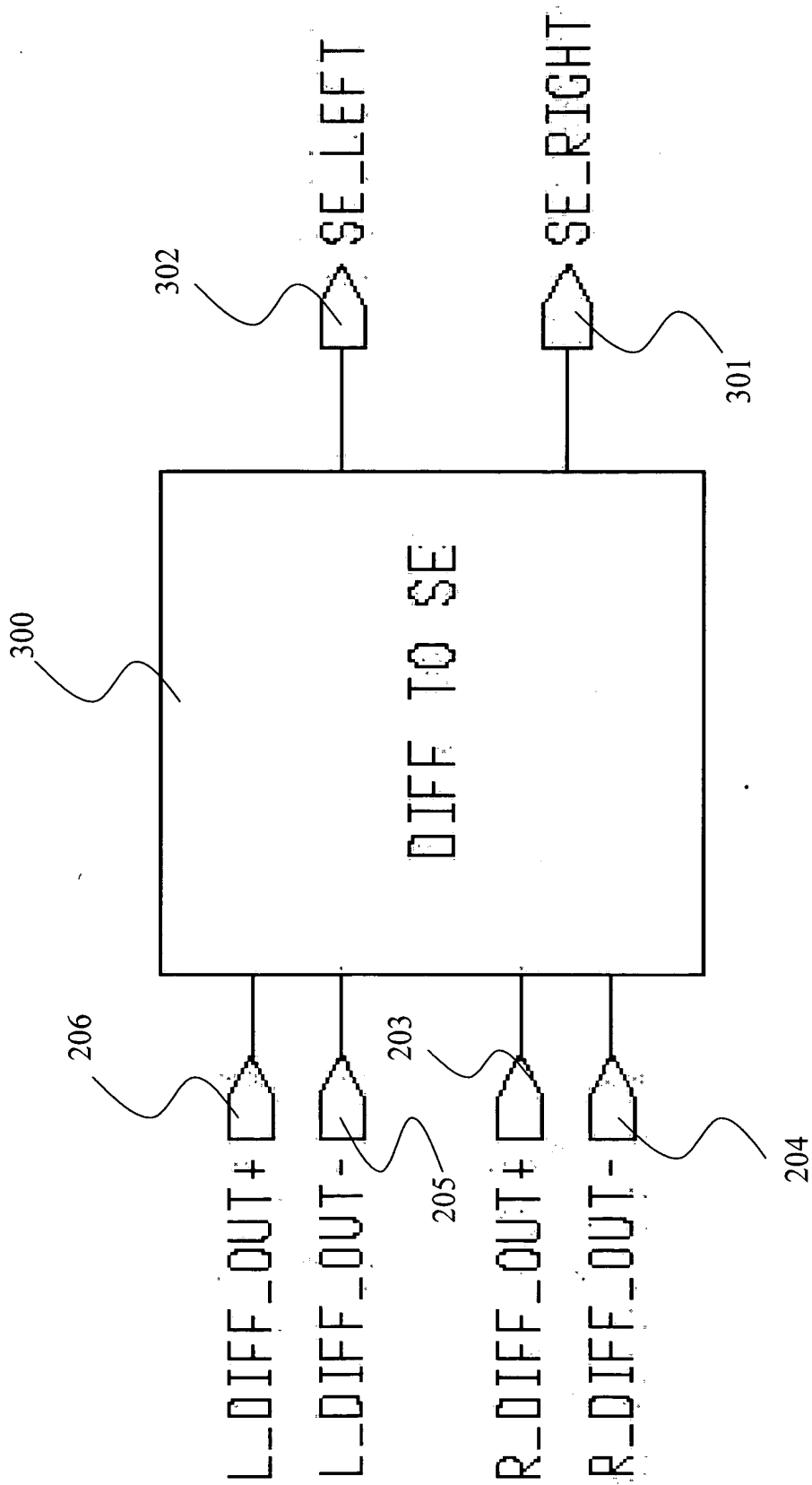


Fig.3

FIG. 3A is a schematic diagram of a differential signal processing circuit 300. The circuit 300 includes a first differential pair of transistors 202 and a second differential pair of transistors 204. The gates of the transistors 202 and 204 are connected to a common gate voltage V_{DD}. The sources of the transistors 202 are connected to ground through a common source resistor 203. The sources of the transistors 204 are connected to ground through a common source resistor 205. The drains of the transistors 202 are connected to a common drain resistor 301. The drains of the transistors 204 are connected to a common drain resistor 302. The circuit 300 is configured to process differential signals L_DIFF_OUT- and R_DIFF_OUT- (labeled 202) and differential signals R_DIFF_OUT+ and L_DIFF_OUT+ (labeled 204). The outputs of the circuit 300 are SE_LEFT and SE_RIGHT.

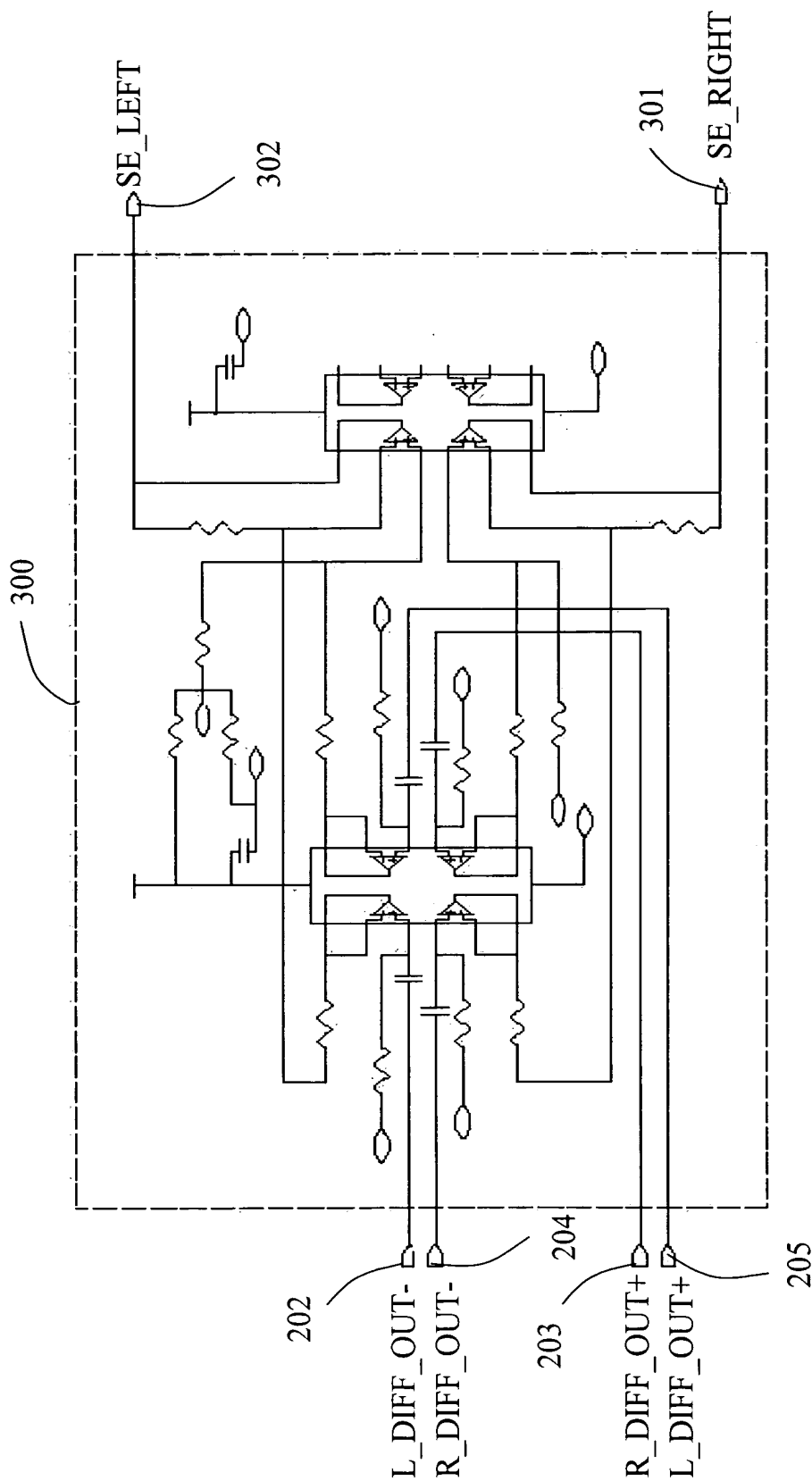


Fig.3A